WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having at least one of four threshold voltages and storing two bits of data;

a plurality of bit lines connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines connected to said plurality of memory cells arranged in the row direction;

a flag cell which is selected at the same time when the memory cells are selected by each of the word lines;

a plurality of data storage circuits which are connected to said plurality of bit lines in a one-to-one correspondence and store data;

a write circuit which writes data on a first page into a plurality of first memory cells selected simultaneously by one of the word lines, then writes data on a second page into said plurality of first memory cells and, when the data on the second page is written, writes data into the flag cell simultaneously selected by the word line, and thereafter writes the data on the first and second pages sequentially into a second memory cell adjacent to the first memory cells

in the bit line direction.

2. The semiconductor memory device according to claim 1, wherein said plurality of memory cells arranged in the column direction are connected in series to form a NAND cell.

3. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having at least one of four threshold voltages and storing two bits of data;

a plurality of bit lines connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines connected to said plurality of memory cells arranged in the row direction;

a plurality of data storage circuits which are connected to said plurality of bit lines in a one-to-one correspondence and store data;

a write circuit which writes data on a first page into a first and a second memory cell adjoining in the bit line, then writes data on a second page into the first memory cell, and thereafter writes the data on the first page into a third memory cell adjacent to the second memory cells in the bit line direction.

4. The semiconductor memory device according to claim 3, further comprising

a flag cell which is selected at the same time when said plurality of memory cells are selected by each of the word lines, wherein

the write circuit, when writing the data on the second page, writes data into the flag cell selected simultaneously by each of the word lines.

5. The semiconductor memory device according to claim 3, wherein said plurality of memory cells arranged in the column direction are connected in series to form a NAND cell.

6. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having one of an 2^n (n is a natural number equal to 2 or more) number of threshold voltages and storing an n number of bits of data;

a plurality of bit lines connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines connected to said plurality of memory cells arranged in the row direction;

a first and a second flag cell which are selected at the same time when the memory cells are selected by the word lines;

a write circuit which divides an n number of pages composed of an n number of bits stored in a plurality

of memory cells selected by one of the word lines into a first and a second area and, when writing data into the first area on a k-th page (2 <= k <= n), writes the data into also the first flag cell and, when writing data into the second area on the k-th page, writes the data into also the second flag cell.

7. The semiconductor memory device according to claim 6, wherein said plurality of memory cells arranged in the column direction are connected in series to form a NAND cell.

8. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having one of an 2^n (n is a natural number equal to 2 or more) number of threshold voltages and storing an n number of bits of data;

a plurality of bit lines connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines connected to said plurality of memory cells arranged in the row direction;

an (n - 1) $\times$ i number of flag cells which are selected at the same time when the memory cells are selected by the word lines;

a write circuit which divides an n number of pages composed of an n number of bits stored in a plurality

of memory cells selected by one of the word lines into an i number (i is a natural number) of areas and, when writing data into the first area on a k-th page ($2 <= k <= n$), writes the data into also the $((k - 2) \times i + 1)$-th flag cell and, when writing data into the i-th area on the k-th page, writes the data into also the $(k - 1) \times i)$-th flag cell.

9. The semiconductor memory device according to claim 8, wherein said plurality of memory cells arranged in the column direction are connected in series to form a NAND cell.

10. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having one of an 2^n (n is a natural number equal to 2 or more) number of threshold voltages and storing an n number of bits of data;

a plurality of bit lines connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines connected to said plurality of memory cells arranged in the row direction;

an i number of flag cells which are selected at the same time when the memory cells are selected by the word lines;

a write circuit which divides an n number of pages

composed of an n number of bits stored in a plurality of memory cells selected by one of the word lines into an i number (i is a natural number) of areas and, when writing data into the first area on a k-th page (2 <= k <= n), writes the data into also the first flag cell and, when writing data into the i-th area on the k-th page, writes the data into also the i-th flag cell.

11. The semiconductor memory device according to claim 10, wherein said plurality of memory cells arranged in the column direction are connected in series to form a NAND cell.

12. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having one of four threshold voltages and storing two bits of data;

a plurality of bit lines, each of which is connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines, each of which is connected to said plurality of memory cells arranged in the row direction;

a first flag cell and a second flag cell which are selected at the same time when the memory cells are selected by each of the word lines; and

a control section which, when writing the data in

a second page composed of the two bits into the memory cells selected by the word line, writes specific data into the first and second flag cells and which, when reading the data in a first page from the memory cells, determines from the data read from the first flag cell whether the second page has been written into the memory cells and which, when reading the data in the second page from the memory cells, determines from the data read from the second flag cell whether the second page has been written into the memory cells.

13. The semiconductor memory device according to claim 12, wherein said plurality of memory cells arranged in the column direction are connected in series to configure a NAND cell.

14. The semiconductor memory device according to claim 12, wherein the first and the second flag cells include a plurality of cells, respectively; and

the control section causes the plurality of cells to store the same logic level in a write operation and decides the output of the first and the second flag cells by a majority of the outputs of the plurality of cells.

15. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having one of a 2^n (n is a natural number equal to 2 or more) number of threshold voltages and

storing an n number of bits of data;

a plurality of bit lines, each of which is connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines, each of which is connected to said plurality of memory cells arranged in the row direction;

an n number of flag cells which are selected at the same time when the memory cells are selected by each of the word lines; and

a control section which, when writing the data in a k-th page (2 <= k <= n) composed of a k number of bits into the memory cells selected by the word line, writes specific data into a k number (2 <= k <= n) of the flag cells and which, when reading the data in an i-th page (i <= n) from the memory cells, determines from the data read from the i-th flag cell whether the k-th page has been written into the memory cells.

16. The semiconductor memory device according to claim 15, wherein said plurality of memory cells arranged in the column direction are connected in series to configure a NAND cell.

17. The semiconductor memory device according to claim 15, wherein the n number of flag cells includes a plurality of cells, respectively, each of cells stores the same logic level; and

the control section causes the plurality of cells

to store the same logic level in a write operation and decides the output of the flag cells by a majority of the outputs of the plurality of cells.

18. A semiconductor memory device comprising:

a memory cell array configured by arranging a plurality of memory cells in a matrix, each of which is capable of having one of a 2^n (n is a natural number equal to 2 or more) number of threshold voltages and storing an n number of bits of data;

a plurality of bit lines, each of which is connected to said plurality of memory cells arranged in the column direction;

a plurality of word lines, each of which is connected to said plurality of memory cells arranged in the row direction;

an (n + (n - 1) + (n - 2) ··· 2) number of flag cells which are selected at the same time when the memory cells are selected by each of the word lines; and

a control section which, when writing the data in a k-th page (2 <= k <= n) composed of a k number of bits into the memory cells selected by the word line, writes specific data into a k number (2 <= k <= n) of the flag cells and which, when reading the data in an i-th page (i <= n) from the memory cells, determines from the data read from the i-th flag cell whether the k-th page has been written into the memory cells.

19. The semiconductor memory device according to claim 18, wherein said plurality of memory cells arranged in the column direction are connected in series to configure a NAND cell.

20. The semiconductor memory device according to claim 18, wherein the $(n + (n - 1) + (n - 2) \cdots 2)$ number of flag cells include a plurality of cells, respectively, each of cells stores the same logic level; and

the control section causes the plurality of cells to store the same logic level in a write operation and decides the output of the flag cells by a majority of the outputs of the plurality of cells.